Brian Benchoff

Hardware / Software Engineer

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Professional Summary

Hardware and embedded systems engineer with over a decade of experience spanning EDA tooling, precision instrumentation, and hardware security. I build the tool when the tool doesn't exist — a GPU-accelerated PCB autorouter that completed designs where commercial routers failed, an open-source FPGA toolchain reverse-engineered from vendor binaries with Ghidra, and data-acquisition systems that cut measurement costs by 90%. Comfortable across the full stack, from low-noise analog front-ends and DFM-ready PCBs to CUDA, embedded Python, and bare-metal firmware. Currently developing automated PCB placement and routing at Flux.ai.

Experience

Flux.ai **San Francisco, CA**
Software Engineer *January 2026-Present*
Developing automated PCB component placement and routing technology for next-generation EDA tools. Building intelligent placement algorithms that optimize for signal integrity, thermal management, and manufacturability constraints. Contributing to cloud-based PCB design platform advancing automated electronic design workflows.

Tampersec **San Francisco, CA**
Hardware Security Engineer *January 2025-December 2025*
Led hardware security development for tamper-evident enclaves for GPUs. Designed and implemented secure hardware architecture for AI model protection in datacenter environments. Developed custom tamper detection circuits. Created specialized test harnesses to validate physical security measures against side-channel and physical attacks.

Span.io **San Francisco, CA**
Electronic Engineer *2022-2024*
Developed novel data acquisition system for thermocouple measurement, reducing costs by 90%. Created comprehensive data acquisition web interface using embedded Python, enabling real-time monitoring for 200+ sensor channels. Designed and fabricated specialized test rigs using KiCad and traditional manufacturing techniques. Created scripted testing procedures with SCPI and PyVisa, Implemented Vehicle-to-Grid (V2G) home backup power solution utilizing Nissan Leaf with CHAdeMO interface. Executed prototype work using CNC (HAAS, Shapeoko), 3D Printing (Stratasys PolyJet, Filament), laser cutting, and fiber laser technologies.

Neusleep **San Francisco, CA**
Hardware Consultant *2021-2022*
Led hardware development for innovative sleep EEG monitoring device. Designed low-noise analog front-end for microvolt-level brainwave signal acquisition. Implemented power-efficient embedded system with BLE connectivity for overnight monitoring. Created DFM-ready PCBs and enclosure designs for production scaling.

Hackaday **Pasadena, CA**
Content Specialist *2011-2021*
Wrote and edited approximately 10,000 technical articles covering embedded systems, electronics design, and hardware engineering. Designed hardware products and reference projects. Built and managed editorial workflows for one of the largest engineering publications online.

Selected Projects

AGaMEMnon: Open-Source FPGA Toolchain *2025-Present*
Reverse-engineered a complete open synthesis, place-and-route, and bitstream toolchain for the AGM AG32 / AGRV2K — a $1 RISC-V microcontroller with an embedded FPGA fabric that ships with no English documentation and only a Windows-only Altera Quartus II clone for tooling. Used Ghidra to decompile the proprietary `af.exe` fabric back-end and recover the full physical bitstream map (554,800 bits across 213 tiles) and complete routing graph. Integrated yosys and nextpnr for open synthesis and routing, and built an open bitstream generator and SWD flasher with no proprietary vendor binary anywhere in the path. Validated byte-for-byte against vendor output and on real silicon, including self-boot from flash. Effectively "Project IceStorm" for a previously closed chip.

OrthoRoute: GPU-Accelerated PCB Autorouter *2025-Present*
Developed GPU-accelerated autorouter implementing PathFinder algorithm for complex PCB designs that exceed capabilities of commercial tools. Created complete KiCad plugin using IPC API, enabling routing of 8M-node graphs (200×200mm, 32-layer boards) in hours versus weeks with traditional tools. Implemented CUDA-based parallel Dijkstra for shortest-path search across Manhattan lattice architecture. Achieved 96.4% routing completion on complex backplane designs where commercial autorouters managed only 4% success rate. Built comprehensive visualization system with real-time routing progress and cloud GPU support for large-scale designs. Designed to handle boards with thousands of nets that cause push-and-shove routers to fail. Open-source project enabling high-density backplane and BGA escape routing for hardware engineers.

Zynq UltraScale+ FPGA / Linux Single-Board Computer *2026*
Designed a production-oriented single-board computer around the AMD/Xilinx Zynq UltraScale+ MPSoC (XCZU2EG, 784-ball 0.8mm-pitch BGA) — quad Cortex-A53 Linux and dual Cortex-R5F real-time cores coupled to programmable logic on one die. Routed DDR4-2400, PCIe Gen2 NVMe, USB 3.0 (4-port hub), Gigabit Ethernet, and DisplayPort directly from the PS-GTR transceivers, and implemented a 10-rail power tree with strict sequencing around a TI TPS6508640 PMIC. Placed 16 independent hardware UARTs in the FPGA fabric for jitter-free hard-real-time I/O, with a baseboard management controller on a spare R5F core for out-of-band console and metrics. Constrained the entire design to a standard 8-layer, non-HDI stackup so it manufactures on a low-cost pooled PCB process — no blind/buried vias or microvias.

Automated Test Equipment Framework - Span.io *2022-2024*
Designed and implemented Python-based automation solution for hardware validation testing. Created instrument drivers for oscilloscopes, power supplies, and electronic loads using PyVisa and SCPI commands. Developed data processing pipelines with Pandas for real-time analysis of 200+ test channels. Implemented object-oriented architecture with class hierarchies for scalable test automation framework.

CAN-Based Automotive Electronics Retrofit *2021-Present*
Converted vintage electric vehicle from relay-based controls to modern embedded CAN architecture. Designed and fabricated custom controller boards for vehicle subsystems. Engineered three interconnected CAN networks with gateway for integrating battery management, motor control, and dashboard systems. Created LED-based digital instrument cluster with custom PCBs and firmware.

Ultra-Low-Cost Linux Embedded Platform *2020-2021*
Developed $15 Linux handheld computer based on Allwinner F1C100s SoC. Created complete hardware design including custom keyboard interface, power management, and display controller. Built working prototype with full Linux functionality and command-line interface. Documented comprehensive BOM optimization strategy for high-volume manufacturing.

Embedded SSL Implementation for Vintage Systems *2025*
Ported modern SSL/TLS stack to classic Mac OS 7/8/9 systems. Overcame severe platform constraints including memory limitations and lack of native entropy sources. Implemented optimization techniques for performance on 68k architecture. Created TCP socket wrapper compatible with legacy networking APIs. Enabled secure modern HTTPS connectivity on 25+ year old computer systems.